DDR3 SDRAM REGISTERED DIMM MODULE,1.5V
8GByte - 1GX72
AVF721GR64F7066G7-BP

FEATURES

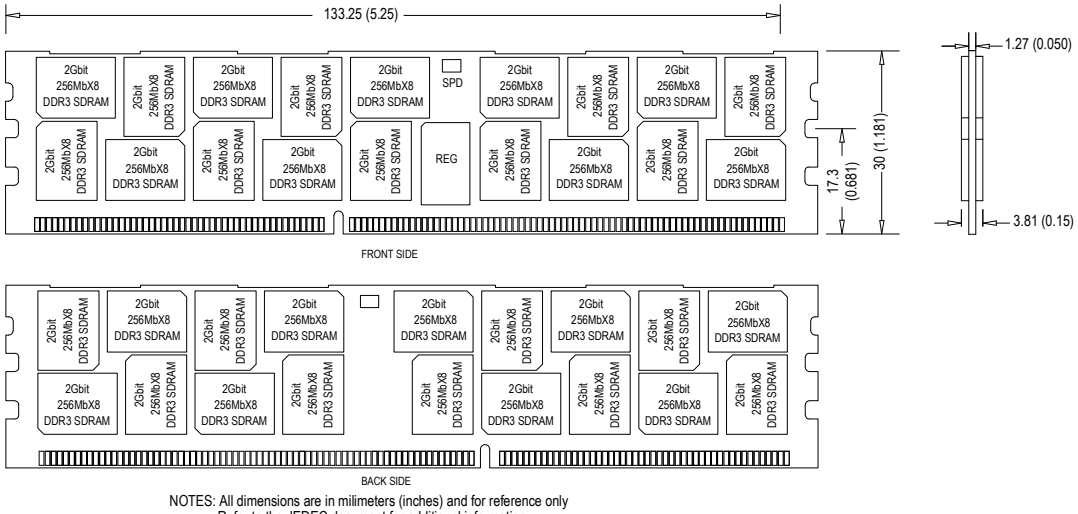
JEDEC DDR2 PC3-8500 1066MT/s, Lead Free, RoHS compliant,

- Clock frequency: 533MHz with CAS latency 7
- 256 byte serial EEPROM
- Data input and output masking
- Programmable burst length: 4, 8
- Programmable burst type: sequential and interleave
- Programmable CAS latency: 7
- Bi-directional Differential Data-Strobe
- Gold card edge fingers
- 8K refresh per 64ms
- Low active and standby current consumption
- On Die Termination (ODT)
- Auto refresh and self refresh capability
- Double-sided module
- 30mm (1.18 inch) height

DESCRIPTION

The AVF721GR64F7066G7-BP is a Registered DDR3 SDRAM DIMM module. This module is JEDEC MO-269 R/C H DDR3 SDRAM Registered DIMM. The module has all the addresses and control signals buffered to reduce capacitive loading. The module utilizes a phase lock loop to reduce the capacitive loading on the clock signals and to synchronize all SDRAM input clocks with the system clock. A 256 byte Temp Sensor serial EEPROM on board can be used to store module information such as timing, configuration, density, etc. as well as to monitor the module temperature and prevent the module from exceeding the maximum operating temperature.
The AVF721GR64F7066G7-BP memory module is 8GByte and organized as 1GX72 ECC array using (36) 256MX8 DDR3 SDRAMs in lead-free FBGA packages.
The module PCB is fabricated using the latest technology design, ten-layer printed circuit board substrate construction with low ESR decoupling capacitors on-board for high reliability and low noise.

PHYSICAL DIMENSIONS



NOTES: All dimensions are in milimeters (inches) and for reference only
Refer to the JEDEC document for additional information.

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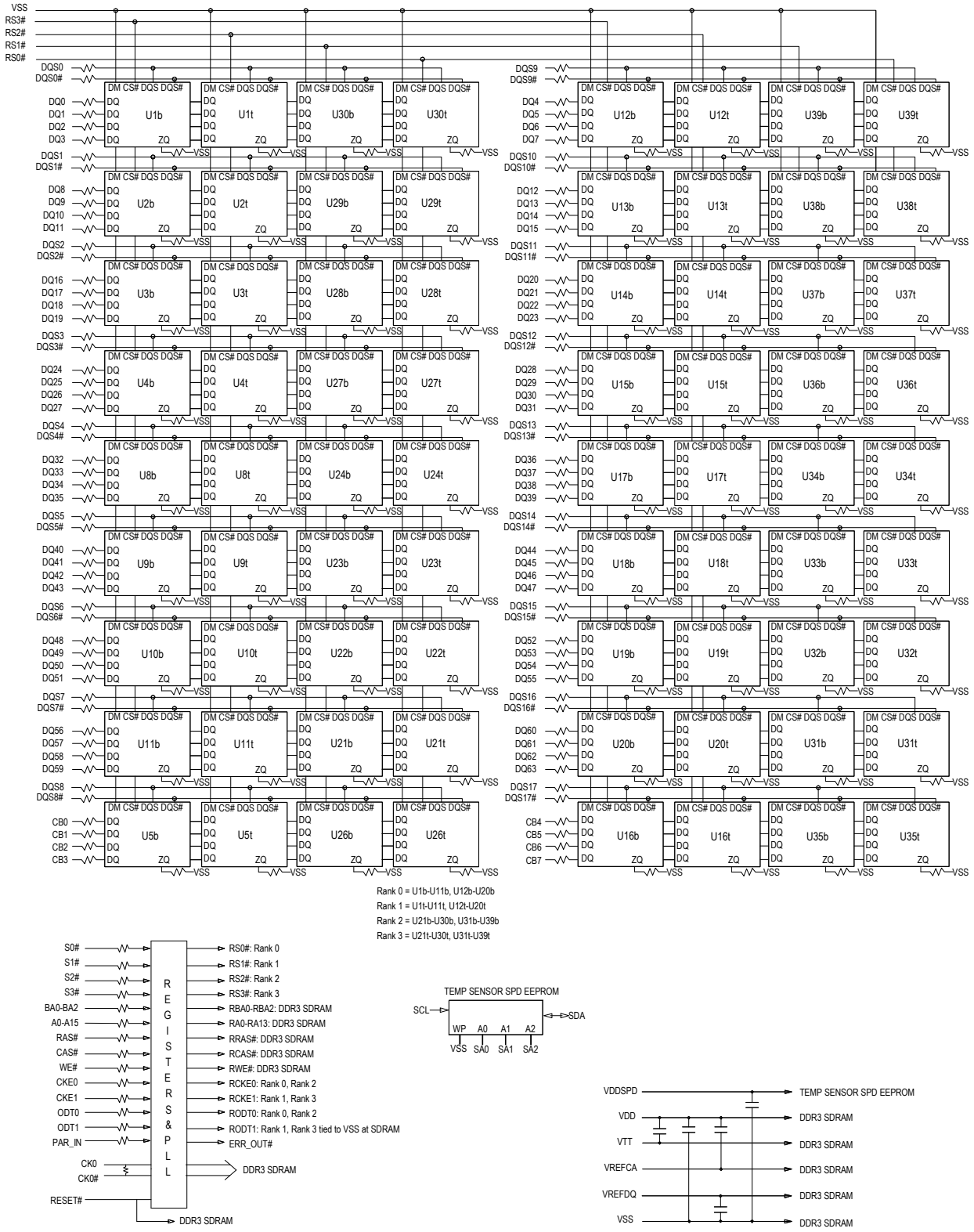
FUNCTIONAL BLOCK DIAGRAM



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MODULE PIN CONFIGURATIONS

PIN	FRONT	PIN	FRONT	PIN	FRONT	PIN	FRONT	PIN	BACK	PIN	BACK	PIN	BACK	PIN	BACK
1	VREF	31	DQ25	61	A2	91	DQ41	121	VSS	151	VSS	181	A1	211	VSS
2	VSS	32	VSS	62	VDD	92	VSS	122	DQ4	152	DQS12	182	VDD	212	DQS14
3	DQ0	33	DQS3#	63	NF	93	DQS5#	123	DQ5	153	DQS12#	183	VDD	213	DQS14#
4	DQ1	34	DQS3	64	NF	94	DQS5	124	VSS	154	VSS	184	CK0	214	VSS
5	VSS	35	VSS	65	VDD	95	VSS	125	DQS9	155	DQ30	185	CK0#	215	DQ46
6	DQS0#	36	DQ26	66	VDD	96	DQ42	126	DQS9#	156	DQ31	186	VDD	216	DQ47
7	DQS0	37	DQ27	67	VREFCA	97	DQ43	127	VSS	157	VSS	187	EVENT#	217	VSS
8	VSS	38	VSS	68	Par_In	98	VSS	128	DQ6	158	CB4	188	A0	218	DQ52
9	DQ2	39	CB0	69	VDD	99	DQ48	129	DQ7	159	CB5	189	VDD	219	DQ53
10	DQ3	40	CB1	70	A10	100	DQ49	130	VSS	160	VSS	190	BA1	220	VSS
11	VSS	41	VSS	71	BA0	101	VSS	131	DQ12	161	DQ17	191	VDD	221	DQ15
12	DQ8	42	DQS8#	72	VDD	102	DQS6#	132	DQ13	162	DQ17#	192	RAS#	222	DQ15#
13	DQ9	43	DQS8	73	WE#	103	DQS6	133	VSS	163	VSS	193	S0#	223	VSS
14	VSS	44	VSS	74	CAS#	104	VSS	134	DQS10	164	CB6	194	VDD	224	DQ54
15	DQS1#	45	CB2	75	VDD	105	DQ50	135	DQS10#	165	CB7	195	ODT0	225	DQ55
16	DQS1	46	CB3	76	S1#	106	DQ51	136	VSS	166	VSS	196	A13	226	VSS
17	VSS	47	VSS	77	ODT1	107	VSS	137	DQ14	167	NC	197	VDD	227	DQ60
18	DQ10	48	VTT	78	VDD	108	DQ56	138	DQ15	168	RESET#	198	NC	228	DQ61
19	DQ11	49	VTT	79	NC	109	DQ57	139	VSS	169	CKE1	199	VSS	229	VSS
20	VSS	50	CKE0	80	VSS	110	VSS	140	DQ20	170	VDD	200	DQ36	230	DQS16
21	DQ16	51	VDD	81	DQ32	111	DQS7#	141	DQ21	171	A15	201	DQ37	231	DQS16#
22	DQ17	52	BA0	82	DQ33	112	DQS7	142	VSS	172	A14	202	VSS	232	VSS
23	VSS	53	NC/Err_Out#	83	VSS	113	VSS	143	DQS11	173	VDD	203	DQS13	233	DQ62
24	DQS2#	54	VDD	84	DQS4#	114	DQ58	144	DQS11#	174	A12	204	DQS13#	234	DQ63
25	DQS2	55	A11	85	DQS4	115	DQ59	145	VSS	175	A9	205	VSS	235	VSS
26	VSS	56	A7	86	VSS	116	VSS	146	DQ22	176	VDD	206	DQ38	236	VDDSPD
27	DQ18	57	VDD	87	DQ34	117	SA0	147	DQ22#	177	A8	207	DQ39	237	SA1
28	DQ19	58	A5	88	DQ35	118	SCL	148	VSS	178	A6	208	VSS	238	SDA
29	VSS	59	A4	89	VSS	119	SA2	149	DQ28	179	VDD	209	DQ44	239	VSS
30	DQ24	60	VDD	90	DQ40	120	VTT	150	DQ29	180	A3	210	DQ45	240	VTT

Pin Names	Description	Pin Names	Description
CK0	Clock Inputs, positive line	ODT0~ODT1	On Die Termination
CK0#	Clock Inputs, negative line	DQ0~DQ63	Data Input/Output
CKE0, CKE1	Clock Enables	CB0~CB7	Data check bits Input/Output
RAS#	Row Address Strobe	DQS0~DSQ17	Data Strobes
CAS#	Column Address Strobe	DQS0#~DQS17#	Data Strobes, negative line
WE#	Write Enable	NF	No Function
S0#~S3#	Chip Selects	NC	No Connect
A0~A15	Address Inputs	NC	No Connect
A10/AP	Address Input/Auto Recharge	VDD	Core Power
BA0~BA2	DDR2 SDRAM Bank Address	VDDQ	I/O Power
SCL	Serial Presence Detect (SPD) Clock Input	VSS	Ground
SDA	SPD Data Input/Output	VREFCA, VREFDQ	Reference Voltage
SA0~SA2	SPD Address	VDDSPD	SPD Power
Par_In	Parity bit for the Address and Control bus	VTT	Termination Voltage
Err_Out#	Parity error found in the Address & Control bus	RESET#	Force all registered outputs LOW

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MODULE SPD TABLE

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NUMBER OF SPD BYTES USED 0x92	SPD REVISON 0x10	DRAM DEVICE TYPE 0x0B	MODULE TYPE (FORM FACTOR) 0x01	SDR DEVICE DENSITY & BANKS 0x02	SDR DEVICE ROW & COLUMN COUNT 0x12	MODULE NOMINAL VDD 0x00	MODULE RANKS & DEVICE DQ COUNT 0x18	ECC TAG & MODULE MEMORY BUS WIDTH 0x0B	FINE TIMEBASE DIVIDEND/ DIVISOR 0x52	MEDIUM TIMEBASE DIVIDEND 0x01	MEDIUM TIMEBASE DIVISOR 0x08	MIN SDRAM CYCLE TIME (t_{CKmin}) 0x0F	BYTE 13 RESERVED 0x00	CAS LATENCIES SUPPORTED (CL4-CL11) 0x1C	CAS LATENCIES SUPPORTED (CL12-CL18) 0x00
1	MIN CAS LATENCY TIME (t_{AAmin}) 0x69	MIN WRITE RECOVERY TIME (t_{WRmin}) 0x78	MIN RAS# TO CAS# DELAY (t_{RCDmin}) 0x69	MIN ROW ACTIVE TO ROW ACTIVE DELAY (t_{RRDmin}) 0x3C	MIN ROW PRECHARGE DELAY (t_{RPmin}) 0x69	UPPER NIBBLE FOR t_{RAS} & t_{RC} 0x11	MIN ACTIVE TO PRECHARGE DELAY (t_{RASmin}) 0x2C	MIN ACTIVE TO ACTIVE/ REFRESH DELAY (t_{RCmin}) 0x95	MIN REFRESH RECOVERY DELAY (t_{RFCmin}) LSB 0x70	MIN REFRESH RECOVERY DELAY (t_{RFCmin}) MSB 0x03	MIN INTERNAL WRITE TO READ CMD DELAY (t_{WTRmin}) 0x3C	MIN INTERNAL READ TO PRECHARGE CMD DELAY (t_{RTPmin}) 0x3C	MIN FOUR ACTIVE WINDOW DELAY (t_{FAWmin}) MSB 0x01	MIN FOUR ACTIVE WINDOW DELAY (t_{FAWmin}) LSB 0x2C	SDR DEVICE OUTPUT DRIVERS SUPPORTED 0x83	SDRAM DEVICE THERMAL & REFRESH OPTIONS 0x8D
2	MODULE THERMAL SENSOR 0x80	SDRAM DEVICE TYPE 0x80	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00
3	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	MODULE HEIGHT (NOMINAL) 0x0F	MODULE THICKNESS (MAX) 0x11	REFERENCE RAW CARD ID 0x05	ADDRESS MAPPING/ MODULE ATTRIBUTES 0x0A
4	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00
5	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00
6	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00
7	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	MODULE MFR ID (LSB) 0x80	MODULE MFR ID (MSB) 0xCE	MODULE MFR LOCATION ID 0x00	MODULE MFR YEAR 0x00	MODULE MFR WEEK 0x00	MODULE SERIAL NUMBER 0x00	MODULE SERIAL NUMBER 0x00	MODULE SERIAL NUMBER 0x00	MODULE SERIAL NUMBER 0x00	CRC 0xAA	CRC 0x16
8	AVANT PART NUMBER 46	AVANT PART NUMBER 37	AVANT PART NUMBER 32	AVANT PART NUMBER 31	AVANT PART NUMBER 47	AVANT PART NUMBER 82	AVANT PART NUMBER 38	AVANT PART NUMBER 34	AVANT PART NUMBER 46	AVANT PART NUMBER 37	AVANT PART NUMBER 30	AVANT PART NUMBER 36	AVANT PART NUMBER 36	AVANT PART NUMBER 47	RESERVED 0x00	RESERVED 0x00
9	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00	RESERVED 0x00
A	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 54	NOT USED 46	NOT USED 31	NOT USED 30	NOT USED 34	NOT USED 35	NOT USED -	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00
B	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00
C	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00
D	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00
E	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00
F	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00

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ABSOLUTE MAXIMUM RATINGS(I)

Item		Symbol	Rating	Unit
Voltage on power supply or any input pin relative to V_{SS}		V_{DDL}, V_{DDQ}, V_{IN}, V_{OUT}	-0.4 ~ 1.975	V
Voltage on power supply or any input pin relative to V_{SS}		V_{DD}	-1.0 ~ 2.3	^{O}C
Storage temperature		t_{STG}	-55 to +100	mA
Operating temperature	1GX72	t_{OPER}	0 to 95	^{O}C

(I) Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. All voltages are referenced to V_{SS} that ties to ground.

DC OPERATING CONDITIONS (II)

Item	Symbol	Min.	Typical	Max.	Unit
Supply voltage	V_{DD}	1.425	1.5	1.575	V
Supply voltage for DLL	V_{DLL}	1.425	1.5	1.575	V
Supply voltage for Output	V_{DDQ}	1.425	1.5	1.575	V
Input Reference Voltage	V_{REF}	0.49*V_{DDQ}	0.5*V_{DDQ}	0.51*V_{DDQ}	mV
Termination Voltage	V_{TT}	V_{REF} - 0.04	V_{REF}	V_{REF}+ 0.04	V

(II) Recommended operating conditions unless otherwise noted. All voltages are referenced to V_{SS} or ground.

DC CHARACTERISTICS (III) (V_{DD} = 1.5 ± 0.1V, V_{SS} = 0V)

				8K REFRESH @ 64ms			
			SYMBOL	CONFIG.	DDR3-1066 with CL = 7		
					TYPICAL	MAX	UNIT
Operating one bank active- precharge current $t_{RC} = t_{RC}$(IDD)			I_{DD0}	1GX72	-	1404	mA
Precharge Power-down Current All banks idle,power-down mode,CKE ≤ V_{IL}(max)			I_{DD2P}	1GX72	-	288	mA
Precharge Standby Current (All bank idle); (CKE is high, CS# is high), $t_{CK} = t_{CK(IDD)}$			I_{DD2N}	1GX72	-	954	mA
Active power-down Current All banks active (CKE is low)			I_{DD3P}	1GX72	-	684	mA
Active Standby Current (Non Power Down Mode) All banks active;CKE is high			I_{DD3N}	1GX72	-	1044	mA
Burst Mode Operating Current All banks Active	(t_{CK} ≥ t_{CK}(min), I_{OL}= 0mA	READ	I_{DD4}	1GX72	-	2394	mA
		WRITE		1GX72	-	2394	mA
Auto Refresh Current All banks Active	t_{RC} = t_{RFC}(min)		I_{DD5}	1GX72	-	3294	mA
Self Refresh Current	CKE ≤ 0.2V	Normal	I_{DD6}	1GX72	-	324	mA
		Low Power		1GX72	-	*	mA

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CAPACITANCE (IV)

PARAMETER	CONFIG.	SYMBOL	MIN	TYP	MAX	UNIT
Input capacitance (A[15:0], BA[2:0], RAS#, CAS#, WE#)	1GX72	C_{I2}	-		TBD	pF
Input capacitance (CKE, CS#)	1GX72	C_{IN3}	-		TBD	pF
Input capacitance (CK, CK#)	1GX72	C_{CK}	-		TBD	pF
Data Input capacitance (DQ, DQS, DQS#, DM)	1GX72	C_{I0}	-		TBD	pF

OPERATING AC CHARACTERISTICS (V)

PARAMETER		SYM	MIN	MAX	UNIT
Clock cycle time	CAS Latency 7	t_{CK}	1.875	<2.5	ns
					ns
Row cycle time		t_{RC}	50.625		ns
Row active time		t_{RAS}	37.5	$9*t_{REF}$	ns
RAS# to CAS# delay		t_{RCD}	13.125		ns
Row precharge time		t_{RP}	13.125		ns
Row active to row active delay		t_{RRD}	7.5		ns
Write recovery time		t_{WR}	15		ns
CAS# to CAS# command delay		t_{CCD}	4		n_{CK}
Clock high level width		t_{CH}	0.43	-	t_{CK}
Clock low level width		t_{CL}	0.43	-	t_{CK}
DQS-out access time from CK or CK#		t_{DQSCK}	-300	+300	ps
Output data access time from CK or CK#		t_{AC}	-300	+300	ps
DQS-DQ skew for DQS & associated DQ signals		t_{DQSQ}	-	150	ps
Read preamble		t_{RPRE}	0.90	-	t_{CK}
Read postamble		t_{RPST}	0.30	-	t_{CK}
Data out high impedance time from CK or CK#		t_{HZQ}	-	300	ps
Write command to first DQS latching transition		t_{DQSS}	WL-0.25	WL+0.25	t_{CK}
DQS-in high level width		t_{DQSH}	0.45	0.55	t_{CK}
DQS-in low level width		t_{DQSL}	0.45	0.55	t_{CK}
Address and control input setup time		t_{IS}	125		ps
Address and control input hold time		t_{IH}	200		ps
Mode register set cycle time		t_{MRD}	4		t_{CK}
DQ & DM set up time to DQS		t_{DS}	30		ps
DQ & DM hold time to DQS		t_{DH}	65		ps
DQ & DM input pulse width		t_{DIPW}	0.35		t_{CK}
Write Preamble		t_{WPRE}	0.90	-	t_{CK}
Write Postamble		t_{WPST}	0.30	-	t_{CK}
DQ hold skew factor		t_{QHS}	0.38	-	t_{CK}
Control & Address input pulse width for each input		t_{IPW}	780	-	ps

V. Values in this table are based on SDRAM component data sheet and may vary from one DRAM manufacturer to another.

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Avant Ordering Guides

AV	F	72	1G	R	64	F	7	066	G	7
INVENTORY	**MOD. TYPE**	**ORG.**	**DENSITY**	**PARITY**	**TYPE**	**VOLT.**	**FEATURE**	**SPEED**	**MODE**	**REV**
AV=AVANT	F = 240-PIN DDR3 DIMM	72=X72	1G= 1024M	R=REGISTERED	64 = 32Mx8x8 (DDR3 SDRAM)	F =1.5V	7 = CAS LATENCY 7	1066MT/s	G=DDR3 SDRAM	REV=7

Other options may be available. Call for specific part number information on options not listed.

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