DDR2 SDRAM UNBUFFERED DIMM MODULE,1.8V
1GByte - 128MX64
AVF6428U52E5667F6

FEATURES

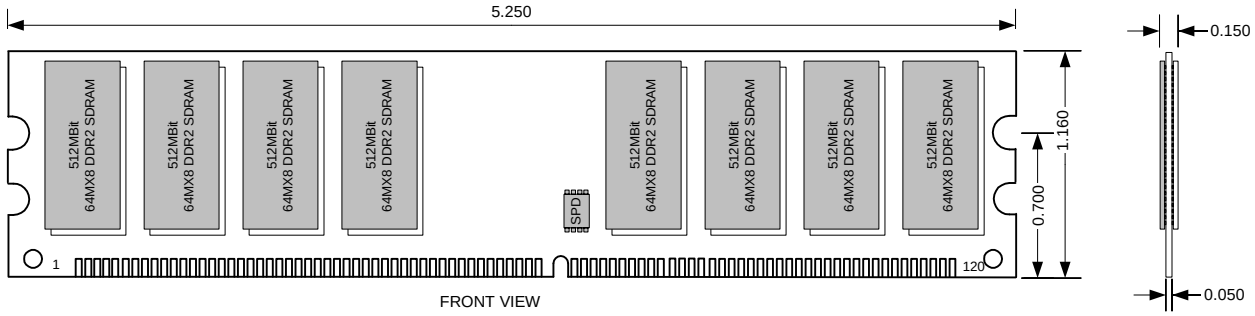
JEDEC DDR2 PC2-5300 667MHz

- Clock frequency: 333MHz with CAS latency 5
- 256 byte serial EEPROM
- Data input and output masking
- Programmable burst length: 4, 8
- Programmable burst type: sequential and interleave
- Programmable CAS latency: 5
- Bi-directional Differential Data-Strobe
- Gold card edge fingers
- 8K refresh per 64ms
- Low active and standby current consumption
- On Die Termination
- Auto refresh and self refresh capability
- Double-sided module
- 1.16 inch height

DESCRIPTION

The AVF6428U52E5667F6 is an Unbuffered DDR2 SDRAM DIMM module. This module is JEDEC Pinout compatible DDR2 SDRAM Unbuffered DIMM. A 256 byte serial EEPROM on board can be used to store module information such as timing, configuration, density, etc.
The AVF6428U52E5667F6 memory module is 1GByte and organized as 128MX64 array using (16) 64MX8 DDR2 SDRAMs in FBGA packages.
The module PCB is fabricated using the latest technology design, six-layer printed circuit board substrate construction with low ESR decoupling capacitors on-board for high reliability and low noise.

PHYSICAL DIMENSIONS



FRONT VIEW

All gray ICs are on the front side, and all white ICs are on the back side of the module

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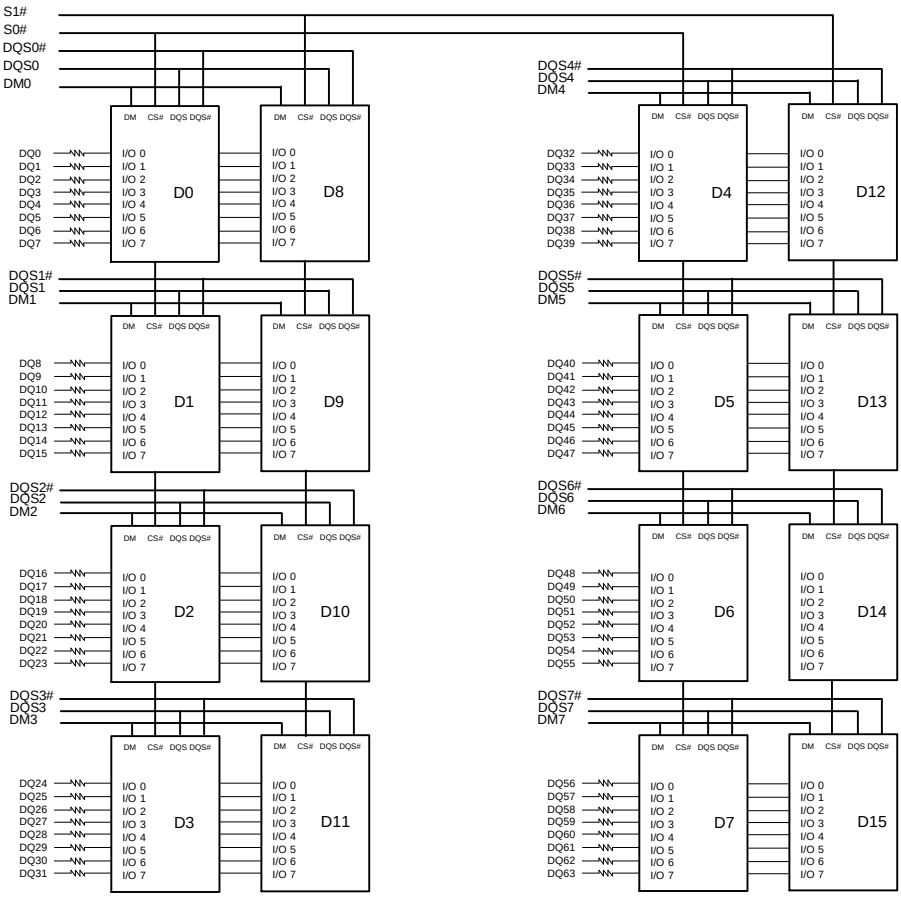
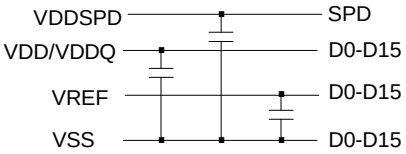
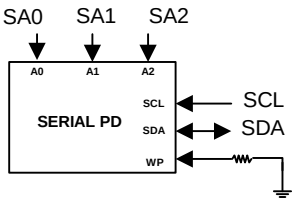
FUNCTIONAL BLOCK DIAGRAM







Notes:
1. DQ, DM, DQS/DQS# resistors are 22 Ohms
2. BAx, Ax, RAS#, CAS#, WE# resistors: 3 Ohms

BA0-BA1 → BA0-BA1: DDR2 SDRAMs D0-D15
A0-A13 → A0-A13: DDR2 SDRAMs D0-D15
RAS# → RAS#: DDR2 SDRAMs D0-D15
CAS# → CAS#: DDR2 SDRAMs D0-D15
CKE0,CKE1 → CKE: DDR2 SDRAMs D0-D7,D8-D15
WE# → WE#: DDR2 SDRAMs D0-D15
ODT0 → ODT: DDR2 SDRAMs D0-D7
ODT1 → ODT: DDR2 SDRAMs D8-D15

CLOCK WIRING	
CLOCK INPUT	**DDR2 SDRAMs**
*CK0 / CK0#	4 DDR2 SDRAMs
*CK1 / CK1#	6 DDR2 SDRAMs
*CK2 / CK2#	6 DDR2 SDRAMs

*Wire per Clock Loading Table/Wiring Diagrams

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MODULE PIN CONFIGURATIONS

PIN	FRONT	PIN	FRONT	PIN	FRONT	PIN	FRONT	PIN	BACK	PIN	BACK	PIN	BACK	PIN	BACK
1	VREF	31	DQ19	61	A4	91	VSS	121	VSS	151	VSS	181	VDDQ	211	DM5
2	VSS	32	VSS	62	VDDQ	92	DQS5#	122	DQ4	152	DQ28	182	A3	212	NC
3	DQ0	33	DQ24	63	A2	93	DQS5	123	DQ5	153	DQ29	183	A1	213	VSS
4	DQ1	34	DQ25	64	VDD	94	VSS	124	VSS	154	VSS	184	VDD	214	DQ46
5	VSS	35	VSS	65	VSS	95	DQ42	125	DM0	155	DM3	185	CK0	215	DQ47
6	DQS0#	36	DQS3#	66	VSS	96	DQ43	126	NC	156	NC	186	CK0#	216	VSS
7	DQS0	37	DQS3	67	VDD	97	VSS	127	VSS	157	VSS	187	VDD	217	DQ52
8	VSS	38	VSS	68	NC	98	DQ48	128	DQ6	158	DQ30	188	A0	218	DQ53
9	DQ2	39	DQ26	69	VDD	99	DQ49	129	DQ7	159	DQ31	189	VDD	219	VSS
10	DQ3	40	DQ27	70	A10/AP	100	VSS	130	VSS	160	VSS	190	BA1	220	CK2
11	VSS	41	VSS	71	BA0	101	SA2	131	DQ12	161	NC	191	VDDQ	221	CK2#
12	DQ8	42	NC	72	VDDQ	102	NC/TEST	132	DQ13	162	NC	192	RAS#	222	VSS
13	DQ9	43	NC	73	WE#	103	VSS	133	VSS	163	VSS	193	S0#	223	DM6
14	VSS	44	VSS	74	CAS#	104	DQS6#	134	DM1	164	NC	194	VDDQ	224	NC
15	DQS1#	45	NC	75	VDDQ	105	DQS6	135	NC	165	NC	195	ODT0	225	VSS
16	DQS1	46	NC	76	S1#	106	VSS	136	VSS	166	VSS	196	A13	226	DQ54
17	VSS	47	VSS	77	ODT1	107	DQ50	137	CK1	167	NC	197	VDD	227	DQ55
18	NC	48	NC	78	VDDQ	108	DQ51	138	CK1#	168	NC	198	VSS	228	VSS
19	NC	49	NC	79	VSS	109	VSS	139	VSS	169	VSS	199	DQ36	229	DQ60
20	VSS	50	VSS	80	DQ32	110	DQ56	140	DQ14	170	VDDQ	200	DQ37	230	DQ61
21	DQ10	51	VDDQ	81	DQ33	111	DQ57	141	DQ15	171	CKE1	201	VSS	231	VSS
22	DQ11	52	CKE0	82	VSS	112	VSS	142	VSS	172	VDD	202	DM4	232	DM7
23	VSS	53	VDD	83	DQS4#	113	DQS7#	143	DQ20	173	NC	203	NC	233	NC
24	DQ16	54	NC	84	DQS4	114	DQS7	144	DQ21	174	NC	204	VSS	234	VSS
25	DQ17	55	NC	85	VSS	115	VSS	145	VSS	175	VDDQ	205	DQ38	235	DQ62
26	VSS	56	VDDQ	86	DQ34	116	DQ58	146	DM2	176	A12	206	DQ39	236	DQ63
27	DQS2#	57	A11	87	DQ35	117	DQ59	147	NC	177	A9	207	VSS	237	VSS
28	DQS2	58	A7	88	VSS	118	VSS	148	VSS	178	VDD	208	DQ44	238	VDDSPD
29	VSS	59	VDD	89	DQ40	119	SDA	149	DQ22	179	A8	209	DQ45	239	SA0
30	DQ18	60	A5	90	DQ41	120	SCL	150	DQ23	180	A6	210	VSS	240	SA1

Pin Names	Description	Pin Names	Description
CK0,CK1,CK2	Clock Inputs, positive line	ODT0~ODT1	On Die Termination
CK0#,CK1#,CK2#	Clock Inputs, negative line	DQ0~DQ63	Data Input/Output
CKE0, CKE1	Clock Enables	DSQ0#~DSQ8	Data Strobes
RAS#	Row Address Strobe	DQS0#~DQS8#	Differential Data Strobes
CAS#	Column Address Strobe	DM0~8	Data Masks/Data Strobes (Read)
WE#	Write Enable		
S0#, S1#	Chip Selects	TEST	Memory bus test tool (Not Connect and Not Useable on DIMMs)
A0~A13	Address Inputs		
BA0, BA1	DDR2 SDRAM Bank Address	VDD	Core Power
SCL	Serial Presence Detect (SPD) Clock Input	VDDQ	I/O Power
SDA	SPD Data Input/Output	VSS	Ground
SA0~SA2	SPD Address	VREF	Input/Output Reference
RESET#	Not used on UDIMM	VDDSPD	SPD Power
NC	No Connect	RFU	Reserved for Future Use

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MODULE SPD TABLE

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NUMBER OF SPD BYTES USED 0x80	TOTAL NUMBER OF SPD BYTES 0x08	FUNDAMENTAL MEMORY TYPE 0x08	# OF ROW ADDRESSES ON ASSY 0x0E	# OF COLUMN ADDRESSES ON ASSY 0x0A	DIMM HEIGHT AND MODULE RANKS 0x61	MODULE DATA WIDTH 0x40	MODULE DATA WIDTH (CONT') 0x00	VOLTAGE INTERFACE LEVEL 0x05	SDRAM CYCLE TIME @ CL 0x30	SDRAM ACCESS FROM CLOCK 0x45	MODULE CONFIG. TYPE 0x00	REFRESH RATE/TYPE 0x82	PRIMARY SDRAM WIDTH 0x08	ERROR CHECKING SDRAM WIDTH 0x00	MINIMUM CLOCK DELAY FOR t_{CCD} 0x00
1	BURST LENGTHS SUPPORTED 0x0C	SDRAM INTERNAL BANKS 0x04	CAS LATENCY SUPPORTED 0x38	MODULE THICKNESS 0x00	DDR2 DIMM TYPE 0x02	SDRAM MODULE ATTRIBUTES 0x00	SDRAM DEVICE ATTRIBUTES 0x03	SDRAM CYCLE TIME @ CL - 1 0x3D	SDRAM ACCESS TIME @ CL - 1 0x45	SDRAM CYCLE TIME @ CL - 2 0x50	SDRAM ACCESS TIME @ CL - 2 0x45	MINIMUM ROW PRECHARGE t_{RP} 0x3C	MINIMUM ROW ACTIVE-ROW ACTIVE, t_{RRD} 0x1E	MINIMUM RAS TO CAS DELAY t_{RCD} 0x3C	MINIMUM RAS PULSE WIDTH t_{RAS} 0x2D	MODULE RANK DENSITY 0x80
2	COMMAND & ADDRESS SETUP TIME 0x20	COMMAND & ADDRESS HOLD TIME 0x27	DATA INPUT SETUP TIME 0x10	DATA INPUT HOLD TIME 0x17	WRITE RECOVERY TIME t_{WR} 0x3C	WRITE TO READ CMD DELAY t_{WTR} 0x1E	READ TO PRECHARGE CMD DELAY t_{RTP} 0x1E	MEM ANALYSIS PROBE 0x00	EXT FOR BYTE 41 & 42 0x00	MIN ACTIVE AUTO REFRESH t_{RC} 0x3C	MIN AUTO/ ACTIVE REFRESH t_{RFC} 0x4B	MAX CYCLE TIME t_{CKMAX} 0x80	MAX DQS-DQ t_{DQSQ} 0x18	MAX READ DATA HOLD SKEW FACTOR t_{QHS} 0x22	PLL RELOCK TIME 0x00	NOT USED 0x00
3	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	SPD REVISION CODE 0x12	CHECK SUM FOR BYTES 0-62 0x2D
4	AVANT JEDEC ID CODE 0X00	AVANT JEDEC ID CODE 0X00	AVANT JEDEC ID CODE 0X00	AVANT JEDEC ID CODE 0X00	AVANT JEDEC ID CODE 0X00	AVANT JEDEC ID CODE 0X00	AVANT JEDEC ID CODE 0X00	AVANT JEDEC ID CODE 0X00	AVANT LOCATION (AUSTIN) 0x00	AVANT PART NUMBER -	AVANT PART NUMBER -	AVANT PART NUMBER 46	AVANT PART NUMBER 36	AVANT PART NUMBER 34	AVANT PART NUMBER 32	AVANT PART NUMBER 38
5	AVANT PART NUMBER 55	AVANT PART NUMBER 35	AVANT PART NUMBER 32	AVANT PART NUMBER 45	AVANT PART NUMBER 35	AVANT PART NUMBER 36	AVANT PART NUMBER 36	AVANT PART NUMBER 37	AVANT PART NUMBER 46	AVANT PART NUMBER -	AVANT PART NUMBER -	REVISION CODE --	REVISION CODE --	MANUFACTURE DATE YEAR	MANUFACTURE DATE WEEK	ASSEMBLY SERIAL NUMBER --
6	ASSEMBLY SERIAL NUMBER --	ASSEMBLY SERIAL NUMBER --	ASSEMBLY SERIAL NUMBER --	NOT USED 54	NOT USED 46	NOT USED 38	NOT USED 30	NOT USED 39	NOT USED 41	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00
7	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	INTEL SPECIFICATION FREQUENCY 0x00	INTEL SPECIFICATION CAS LATENCY 0x00
8	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00
9	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00
A	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00
B	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00
C	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00
D	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00
E	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00
F	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00	NOT USED 0x00

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ABSOLUTE MAXIMUM RATINGS(I)

Item		Symbol	Rating	Unit
Voltage on power supply or any input pin relative to V_{SS}		V_{DDL}, V_{DDQ}, V_{IN}, V_{OUT}	-0.5 ~ 2.3	V
Voltage on power supply or any input pin relative to V_{SS}		V_{DD}	-1.0 ~ 2.3	^{O}C
Storage temperature		t_{STG}	-55 to +100	mA
Operating temperature	128Mx64	t_{OPER}	0 to 95	^{O}C

(I) Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. All voltages are referenced to V_{SS} that ties to ground.

DC OPERATING CONDITIONS (II)

Item	Symbol	Min.	Typical	Max.	Unit
Supply voltage	V_{DD}	1.7	1.8	1.9	V
Supply voltage for DLL	V_{DLL}	1.7	1.8	1.9	V
Supply voltage for Output	V_{DDQ}	1.7	1.8	1.9	V
Input Reference Voltage	V_{REF}	0.49*V_{DDQ}	0.5*V_{DDQ}	0.51*V_{DDQ}	mV
Termination Voltage	V_{TT}	V_{REF} - 0.04	V_{REF}	V_{REF}+ 0.04	V

(II) Recommended operating conditions unless otherwise noted. All voltages are referenced to V_{SS} or ground.

DC CHARACTERISTICS (III) (V_{DD} = 1.8 ± 0.1V, V_{SS} = 0V)

			8K REFRESH @ 64ms				
			SYMBOL	CONFIG.	667MHz Speed with CL = 5		
					TYPICAL	MAX	UNIT
Operating one bank active- precharge current $t_{RC} = t_{RC}$(IDD)			I_{DD0}	128Mx64	-	1000	mA
Precharge Power-down Current All banks idle,power-down mode,CKE ≤ V_{IL}(max)			I_{DD2P}	128Mx64	-	128	mA
Precharge Standby Current (All bank idle); (CKE is high, CS# is high), $t_{CK} = t_{CK(IDD)}$			I_{DD2N}	128Mx64	-	640	mA
Active power-down Current All banks active (CKE is low)			I_{DD3P}	128Mx64	-	480	mA
Active Standby Current (Non Power Down Mode) All banks active;CKE is high			I_{DD3N}	128Mx64	-	760	mA
Burst Mode Operating Current All banks Active	($t_{CK} \geq t_{CK}$(min), I_{OL}= 0mA	READ	I_{DD4}	128Mx64	-	1480	mA
		WRITE		128Mx64	-	1440	mA
Auto Refresh Current All banks Active	$t_{RC} = t_{RFC}$(min)		I_{DD5}	128Mx64	-	1520	mA
Self Refresh Current	CKE ≤ 0.2V	Normal	I_{DD6}	128Mx64	-	128	mA
		Low Power		128Mx64	-	*	mA

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CAPACITANCE (IV)

PARAMETER	CONFIG.	SYMBOL	MIN	TYP	MAX	UNIT
Input capacitance (A[13:0], BA[1:0], RAS#, CAS#, WE#)	128Mx64	C_{I2}	-		42	pF
Input capacitance (CKE, CS#)	128Mx64	C_{IN3}	-		42	pF
Input capacitance (CK, CK#)	128Mx64	C_{CK}	-		28	pF
Data Input capacitance (DQ, DQS, DQS#, DM)	128Mx64	C_{I0}	-		9	pF

OPERATING AC CHARACTERISTICS (V)

PARAMETER		SYM	MIN	MAX	UNIT
Clock cycle time	CAS Latency 5	t_{CK}	3	8	ns
	CAS Latency 4		3.75	8	ns
Row cycle time		t_{RC}	54		ns
Row active time		t_{RAS}	39	70K	ns
RAS# to CAS# delay		t_{RCD}	15		ns
Row precharge time		t_{RP}	15		ns
Row active to row active delay		t_{RRD}	10		ns
Write recovery time		t_{WR}	15		ns
CAS# to CAS# command delay		t_{CCD}	2		t_{CK}
Clock high level width		t_{CH}	0.45	0.55	t_{CK}
Clock low level width		t_{CL}	0.45	0.55	t_{CK}
DQS-out access time from CK or CK#		t_{DQSCK}	-400	+400	ps
Output data access time from CK or CK#		t_{AC}	-450	+450	ps
DQS-DQ skew for DQS & associated DQ signals		t_{DQSQ}	-	240	ps
Read preamble		t_{RPRE}	0.90	1.10	t_{CK}
Read postamble		t_{RPST}	0.40	0.60	t_{CK}
Data out high impedance time from CK or CK#		t_{HZQ}	-	t_{AC} max	ps
Write command to first DQS latching transition		t_{DQSS}	-0.25	+0.25	t_{CK}
DQS-in high level width		t_{DQSH}	0.35	-	t_{CK}
DQS-in low level width		t_{DQSL}	0.35	-	t_{CK}
Address and control input setup time		t_{IS}	200		ps
Address and control input hold time		t_{IH}	275		ps
Mode register set cycle time		t_{MRD}	2		t_{CK}
DQ & DM set up time to DQS		t_{DS}	100		ps
DQ & DM hold time to DQS		t_{DH}	175		ps
DQ & DM input pulse width		t_{DIPW}	0.35		t_{CK}
Write Preamble		t_{WPRE}	0.35	-	t_{CK}
Write Postamble		t_{WPST}	0.40	0.60	t_{CK}
DQ hold skew factor		t_{QHS}	-	340	ps
Control & Address input pulse width for each input		t_{IPW}	0.60	-	t_{CK}

V. Values in this table are based on SDRAM component data sheet and may vary from one DRAM manufacturer to another.

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Avant Ordering Guides

AV	F	64	28	U	52	E	5	667	F	6
INVENTORY	**MOD. TYPE**	**ORG.**	**DENSITY**	**PARITY**	**TYPE**	**VOLT.**	**FEATURE**	**SPEED**	**MODE**	**REV**
AV=AVANT	F=240-PIN DDR2 DIMM	64=x64	28 = 128M	U = Unbuffered	52 = 8Mx8x8 (DDR2 SDRAM)	E=1.8V	5 = CAS LATENCY 5	667MHZ	F=DDR2 SDRAM	REV=6

Other options may be available. Call for specific part number information on options not listed.

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